

**REMARKS**

The specification has been amended to correct minor clerical errors and to employ more idiomatic English. No new matter has been entered.

Claims 1 and 2 have been amended to address the §112 rejections, and to clarify the invention.

The art rejection is respectfully traversed.

In rejecting the claims as obvious from Matsuda (U.S. Patent No. 6,037,245), the Examiner refers to Matsuda as teaching a process of forming a pattern in a semiconductor device fabrication process in which first and second photoresist layers are applied, exposed and etched. However, Matsuda fails to teach forming the first and second resist layers where the second resist layer has a higher resistance against dry-etching than the first layer, as required by Applicant's independent claim 1, or the advantages resulting therefrom in terms of, for example, increased accuracy and the reduced ashing steps. Moreover, Matsuda nowhere teaches or suggests using the resist pattern as a mask, as required by Applicant's claim 1. Accordingly, neither claim 1, nor any of the claims dependent thereon, can be said to be anticipated by or obvious from Matsuda.

New claims 18-20 have been added to further scope the invention and are allowable for the same reasons above adduced relative to claim 1, as well as for their own additional limitations.

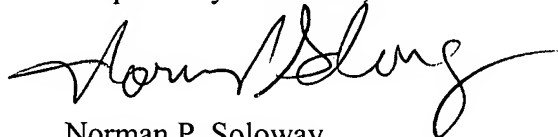
Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

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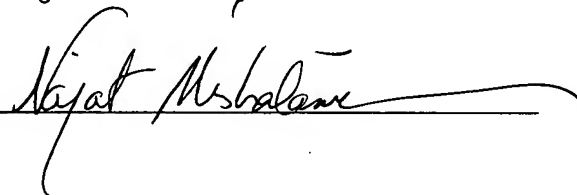
Respectfully submitted,



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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 7, 2004, at Tucson, Arizona.

By 

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